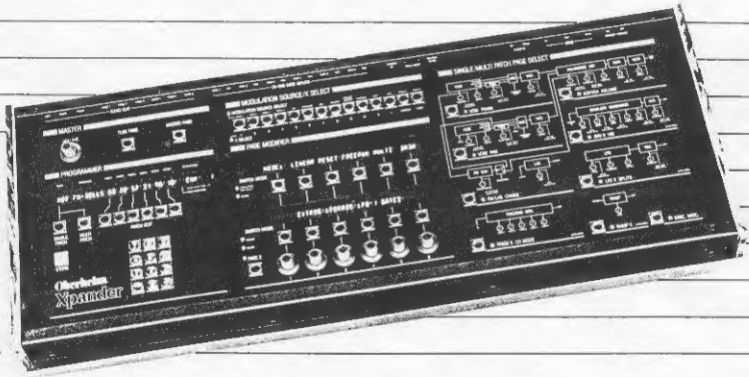
SERVICE MANUAL

Part Number 950037



Oberheim

Xpander

A Division of ECC Development Corporation

Xpander
Service Manual

First Edition

Part Number 950037

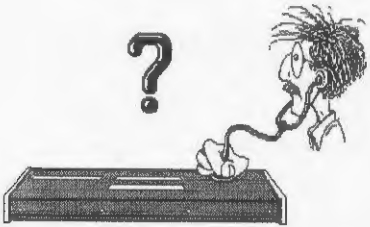
Oberheim
A Division of ECC Development Corporation
11650 W. Olympic Blvd., Los Angeles, CA 90064

INTRODUCTION

The design philosophy behind the Xpander was to include all the features of a modular synthesizer in a programmable and easy to use instrument. At the same time, reliability, accuracy, and ease of servicing have been a prime concern through every step of the design. The result is the most complete and accurate analog polyphonic synthesizer ever built, despite the inclusion of 6 trimmers.

Besides the schematics and the calibration procedure, this manual includes basic explanations of some of the Xpander's circuits. We hope that despite their simplicity they will lead you to a better understanding of the Xpander and therefore to faster and easier servicing.

All of the Xpander general operation procedures are contain in the Xpander Owner's Manual.

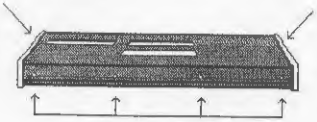


When ordering spare parts from Oberheim Electronics, always indicate the **Oberheim part number** (see the Oberheim part number cross reference at page 60). This will speed up your order and avoid possible errors.

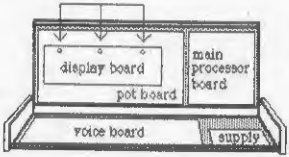
Warning: To avoid loss of data, save customer's data on tape prior to any technical servicing.

MECHANICAL ASSEMBLY

To access the inside of the Xpander you must:
-- Remove the 4 screws along the front of the unit.
-- Remove the top screw on the right and left wooden end-bells.
The whole front panel can now hinge back.



To access the vacuum fluorescent displays (alpha numeric displays), you must remove the three screws along the top of the display board. The display board can now hinge down.



XPANDER CIRCUITRY OVERVIEW

The key to the outstanding performance and features of the Xpander is the intensive use made of its two built-in microprocessors.

The first microprocessor is called the main processor and is located on the processor board. Its main tasks are :

-- Collecting and processing information coming from the front panel controllers (encoders and switches).

-- Collecting and processing information coming from the outside of the Xpander through MIDI or control input jacks (CVs and GATES, PEDAL etc.).

-- Controlling the displays (alpha numeric and LEDs).

-- Storing sound parameters in battery back up memory.

-- Receiving and sending cassette data.

-- Controlling the sound parameters of the voices.

The second microprocessor, called the voice processor, is located on the voice printed circuit board.

The voice processor receives the sound parameter data from the main processor (VCO frequency, LFO 2 speed, envelope 3 attack time etc.) and generates all the modulations and controls that drive the analog circuitry. It also performs a number of automatic calibrations and corrections which insure the accurate behavior of the analog circuitry of each voice.

The Xpander's circuitry is spreed on five printed circuit boards.

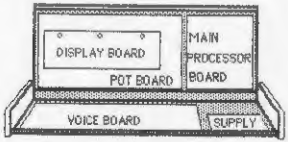
-- The processor board

-- The pot board

-- The display board

-- The voice board

-- The power supply board



THE PROCESSOR BOARD:

The processor board is located in the upper right corner (when the unit is open). It holds :

--The 16 MHZ clock.
--The main processor.
--The power up/down detection circuit (PUP).
--The battery back up memory for the program retention as well as the battery itself.
--The MIDI in and out circuitry.
--The cassette in and out circuitry.
--Some of the LED latches.
--The analog noise generator.

THE POT BOARD:

The pot board is located in the upper left. It holds:

--The switch decoding circuit.
--The external CVs and gates circuit.
--The pedal circuit.
--The step encoder decoding circuit.
--Some of the LED latches.
--The audio master volume control.

THE DISPLAY BOARD:

The display board is located on top of the pot board. It holds:

--The decoding for the display's digits.
--The high voltage buffer for the diplays.
--The three 40-digit vacuum fluorescent display tubes.

THE VOICE BOARD:

The voice board is located on the bottom left. It holds:

--The processor interface circuit.
--The voice processor and its ROM and RAM.
--The DAC.
--The analog circuitry for the 6 voices.
--The panning circuit.

THE POWER SUPPLY:

The power supply is located on the bottom right.

THEORY OF OPERATION:

The following chapter provides information only on the parts of the Xpander's circuitry which present some originality and innovation. A basic knowledge of synthesizer electronic circuits is required.

SWITCHING POWER SUPPLY:

In order to decrease the heat dissipation without using bulky heat sinks, the Xpander uses a switching power supply which operates as follows:

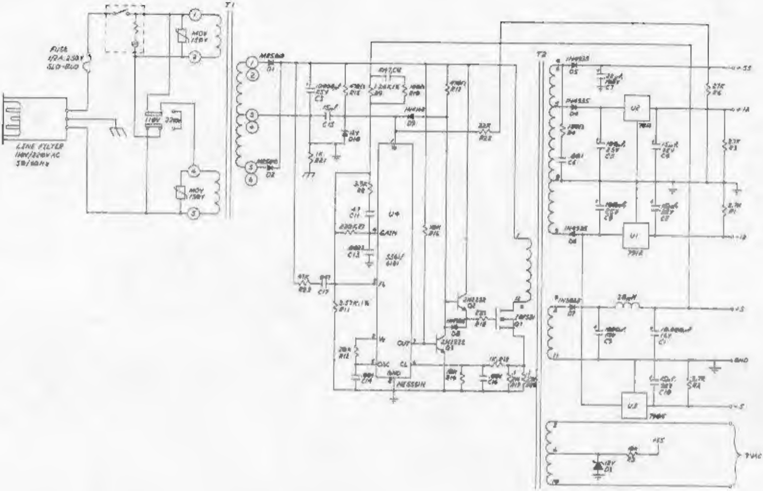
The line AC voltage is first stepped down, rectified and filtered by T1, D1, D2 and C3 to produce a low DC voltage (approximately 13 volts). This DC voltage is then chopped (switched) by Q1 at a frequency of approximately 30 KHz to produce a variable pulse width wave. This pulse is applied through the primary of the step transformer T2 which provides in return on its secondary windings all the different voltages used in the Xpander. Those AC voltages (30 KHz frequency) are then rectified (D5,D4,D6,D7), filtered (C7,C5,C8,C9,C1,C10) and if necessary, regulated (U2,U1,U3). Finally, the 5 volt supply is fed back into the "oscillator/pulse width modulator" integrated circuit U4 to modulate the pulse width and provide the basic voltage regulation.

The advantage of this method over the conventional voltage regulation scheme lies in the fact that the regulation is achieved by modulating the width of a pulse wave rather than the resistance of a transistor. The modulated pulse turns on and off the power MOS transistor Q1 which will therefore always be in one of the two following states:

ON : voltage across =0 , drain current = max ---> power=0

OFF: voltage across =max , drain current = 0 ---> power=0

As there is no power across the transistor in both states, there is no heat production.


FUSE
LINE FILTER
MOV
T1
T2
U4
U1
U2
U3
GND

DUAL MICROPROCESSOR INTERFACE:

The two microprocessors of the Xpander are running two different programs in parallel; the main processor is mainly in charge of collecting and processing the information of the front panel, and the voice processor generates the envelopes, LFOs, LAG etc. for the 6 voices. At some point it is necessary for the main processor to write a new sound parameter into the voice processor memory (for example, a new speed value for an LFO or a new note value for a voice). This is done through the microprocessor interface circuitry located on the voice board. This circuitry includes: one bidirectional octal buffer (U904), four 3-state buffers (U903, U902, U901, U916), 3 OR gates (U906) and a transistor (Q901).

Every time the main processor has to change a parameter in the voice processor memory, the following sequence of events occurs:

A) The main processor sets the HALTREQ* (halt request) line LOW (pin 10 of U906 OR gate).

B) If the voice processor did not previously set the HALTDS (halt disabled) line high, the voice processor will halt, meaning that it will:

1) Stop execution of its program after completion of the current instruction.
2) Put its data and address lines in high impedance state.
3) Set high the BA line (bus available).

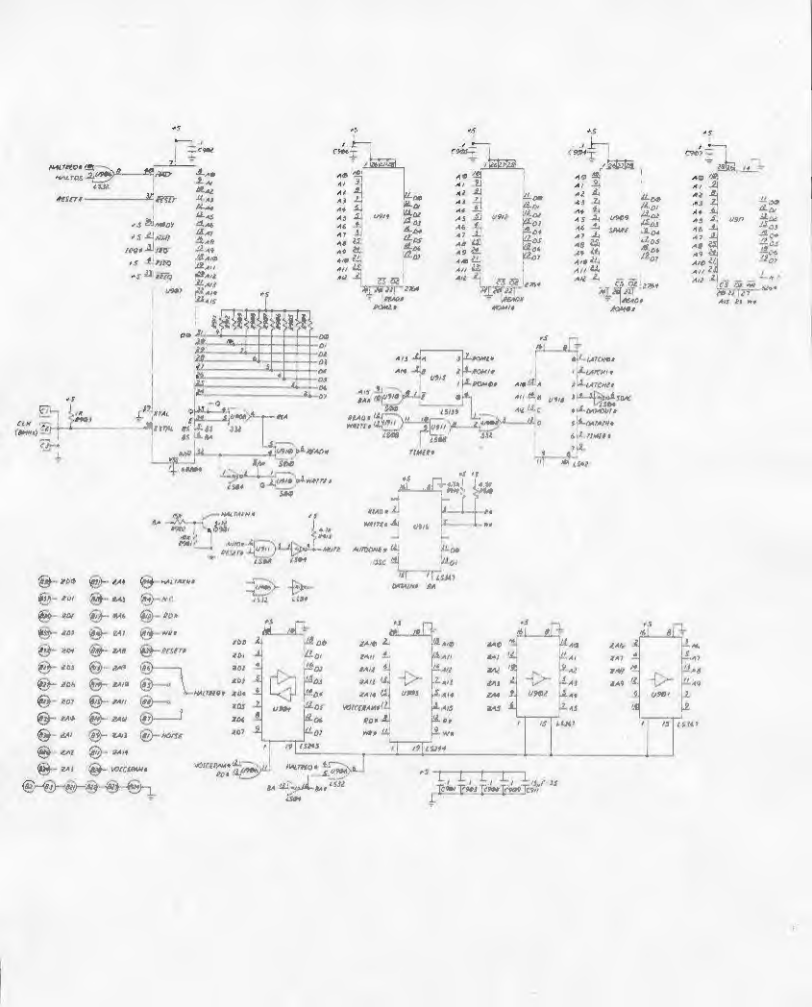
C) BA high will do two things:

1) Through U904,U903,U902,U901 it will connect the data and address lines of the main processor to the data and address line of the voice processor and through U903 and U916 it will switch the read and write lines of the voice processor for the read and write lines of the main processor.
2) Set the HALTAKN* (halt aknowledge) line low (Q901 collector).

D) By sensing the HALTAKN* line low, the main processor knows that its data and address lines are now connected to the voice processor memory and that it can therefore read from or write into it.

E) When the data transfer is completed, the main processor sets the HALTREQ* line high again, allowing the voice processor to retrieve control of its bus and resume its operation.

NOTE: If during normal operation (no tuning or cassette transfer) the voice processor does not aknowledge a halt request in less than 1 second, the main processor will sense a malfunction and will display: "VOICE PROCESSOR MALFUNCTION".

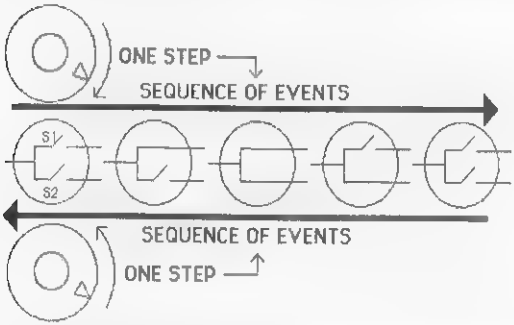


STEP ENCODERS:

In order to facilitate parameter edition, the Xpander uses six step encoders located at the bottom of the PAGE MODIFIER section

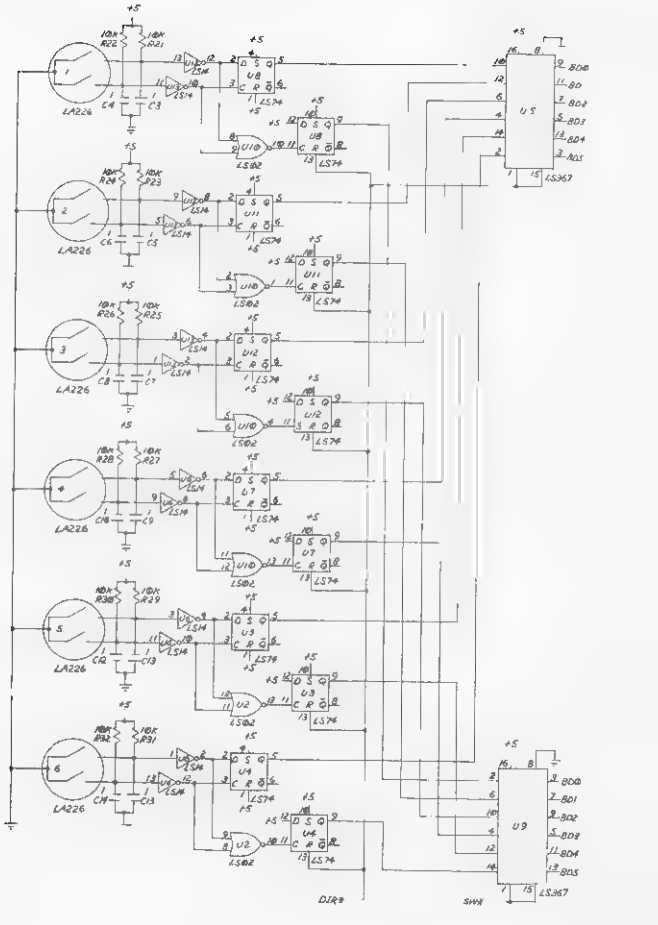
Step encoders, from the outside, seem to behave and look like 360 degree potentiometers, but in practice operate in a completely different way

They are internally made of two switches and a toothed wheel with 30 teeth Each of the steps (clicks) generates a sequence of closing and opening for the two switches s1 and s2 The sequence will be different according to the direction of the rotation



Each encoder is connected to decoding circuitry that automatically senses every step and its direction

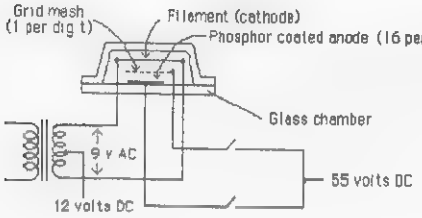
Consider the circuitry of the encoder number 1 where R22, R21 C3 and C4 debounce the encoder switches Whenever one of the 2 switches closes, pin 10 of the NOR gate U10 will go low until both switches are open again This low to high transition will latch a high level on pin 9 of U8 indicating that the sequence of events for one step has been completed The main processor can read the status of the six encoders through the tri-state gate U9 In parallel, pin 5 of J8 is set high or low according to the direction of the rotation of the encoder The main processor can read the direction through the tri-state gate U5 Note that when U5 is enabled (DIR* is low) all the step sensor latches are reset


+5
10K R22
10K R21
LA226
C4
C3
U1 LS14
U8 LS74
U10 LS02
U5 LS367
BD0
BD1
BD2
BD3
BD4
BD5
10K R24
10K R23
C6
C5
U11
10K R26
10K R25
C8
C7
U12
10K R28
10K R27
C10
C9
U7
10K R30
10K R29
C12
C13
U3
U2
10K R32
10K R31
C14
U4
U9
DIR
SW1

VACUUM FLUORESCENT DISPLAYS:

The three 40-digit vacuum fluorescent displays (VFD) and their drivers are located on the display board.

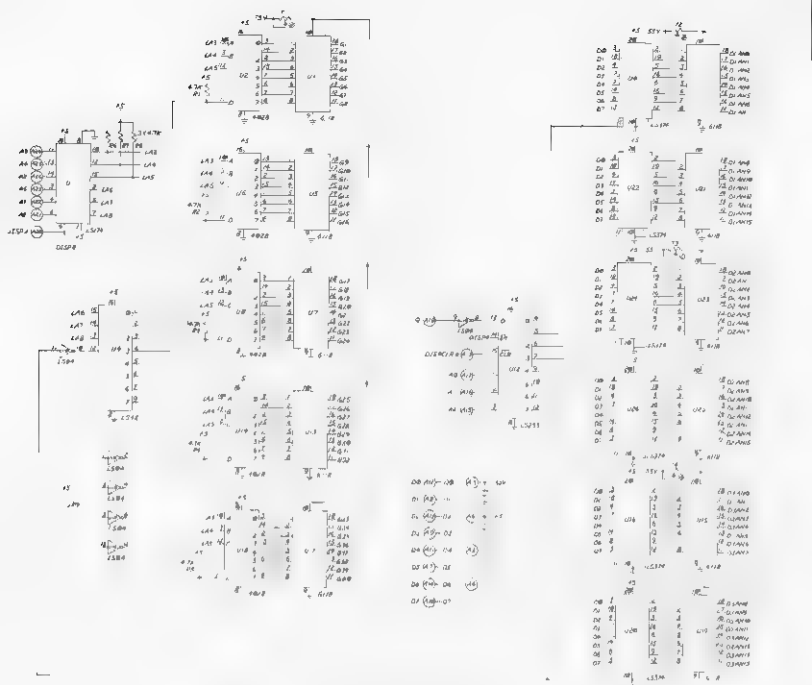
The VFD consists of three basic electrodes in an evacuated glass chamber (see fig below). The electrodes are the cathode, grid and anode. The cathode is a small diameter oxide-coated tungsten filament running across the length of the display and is directly heated by an AC current. The grid is a thin metal screen mesh covering the area over each digit. The anode is coated with phosphor and is arranged in 16 independent segments for each digit.

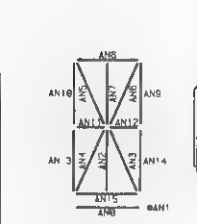


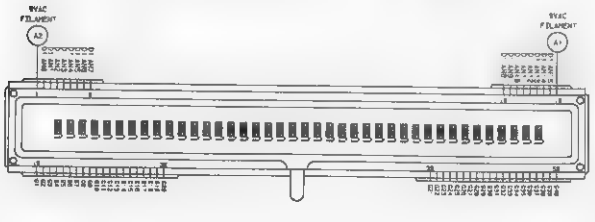
When a positive voltage is applied to the grid and anode, the resultant electrical field will accelerate electrons toward the grid. Since the grid is a mesh, most of the electrons will pass through the grid. Electrons that have passed the grid are further accelerated toward the anode, but collide with the phosphor before reaching it. The electrons deposit most of their energy on the phosphor. This transfer of energy excites the phosphor, which emits a rich blue-green light.

All the identical segments of the 40 digits are connected together and brought out on pins AN0 through AN15 (for example, all the underline segments are connected to pin AN0). The 40 grids are individualy available on pin G1 through G40.

The VFD drive circuitry is shown on the next page. On the left side are the grid drivers (U11,9,1,2,5,6,7,8,13,14,17,18), and on the right side are the anode drivers (U12,3,4,21,22,23,24,25,26,15,16,19,20). Under the control of the main processor, the grids of the 3 VFD are sequentially turned on one at a time from G1 through G40. Before turning on the next grid, a new combination of anodes, determining the displayed pattern, is latched for each of the 3 VFDs.



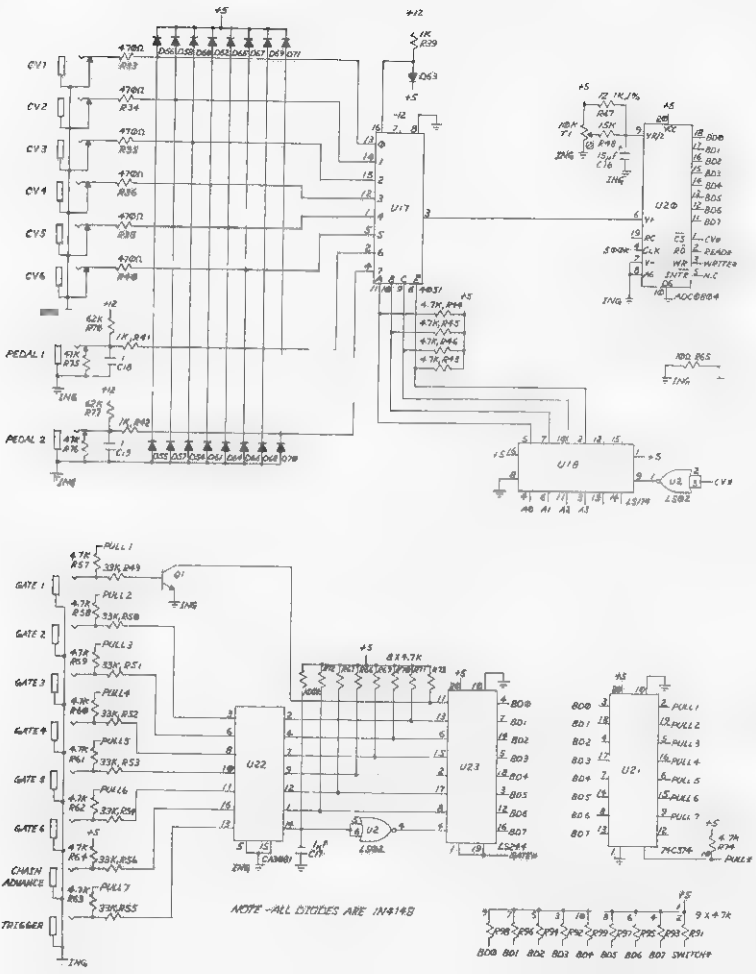

AN8
AN10
AN9
AN11
AN12
AN13
AN14
AN15
AN0
AN1


9VAC
FILAMENT
A2
9VAC
FILAMENT
A1

GATE AND CV INPUTS:

The six gates chain advance and trigger signals are buffered through Q1 and the seven transistors contained in U22. The eight resistors R57 through R63 are either pulling up or down the input according to the state of the lines PULL1 through PULL7. These lines will be set low if the corresponding gate polarity is set for + and set high if the gate polarity is set for -. This setup automatically forces an unused input into its passive state.

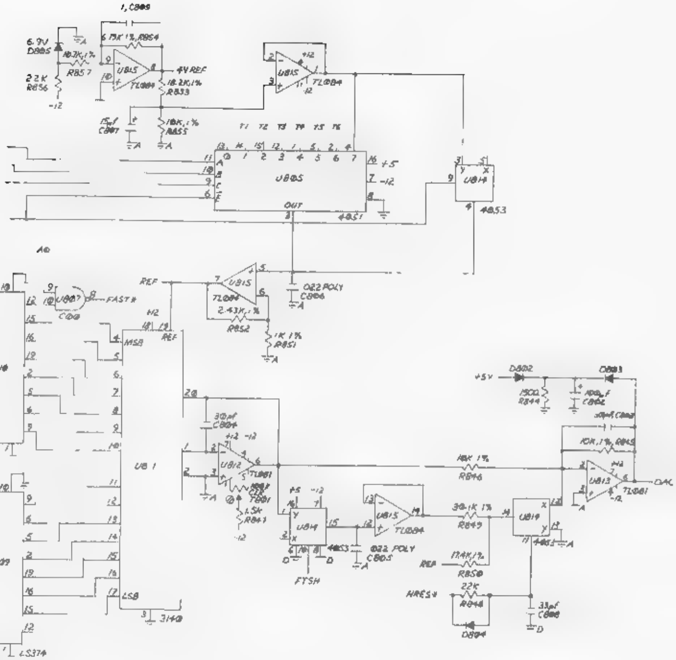
The CV and pedal voltages present on the rear panel jacks are multiplexed through U17 under the control of the main processor. Each of the voltages are then sequentially converted to an 8-bit digital value by the analog to digital converter U20. Only the six most significant bits are used. The diodes D55 through D71 limit the range of the input voltage to 0 and 5.6 volts.


CV1
CV2
CV3
CV4
CV5
CV6
PEDAL 1
PEDAL 2
U17
U18
U2Ø
U22
U23
U21
Q1
GATE 1
GATE 2
GATE 3
GATE 4
GATE 5
GATE 6
CHAIN ADVANCE
TRIGGER
NOTE -ALL DIODES ARE IN4148
9 X 4.7K
SWITCH+

VCO TEMPERATURE COMPENSATION:

Each 3374 dual VCO chip used on the analog voices includes a temperature sensor circuit that provides on pin 10 a voltage proportional to the chip internal temperature These voltages are filtered and buffered on each voice by CX35 and JX05 The six voltages are then routed to U805 in the DAC area The circuitry composed of U805, U814, U815 allows selection, under the control of the main processor, of one of the six temperature reference voltages or a fixed reference to be the DAC reference Because the DAC used in the Xpander is a multiplying DAC, the voltage on the output of the DAC circuitry is directly proportional to the reference when the DAC loads a sample and hold controlling the frequency of a VCO, the temperature reference voltage of this VCO will be used as reference for the DAC Therefore , if the internal temperature of a VCO rises its frequency voltage control will raise proportionally, keeping the resulting frequency stable When the DAC loads the sample and hold of a non-temperature dependant parameter (Pulse width for example) the fixed voltage reference will be used as DAC reference

The temperature stability of the VCO s frequency resulting from this method is far better than the one achieved with the CEM 3340 VCO chip because the correction scaling is performed by the multiplying DAC rather than by the analog multiplier built into the CEM 3340



1, C809
6.9V D805
6.19K 1%, R854
10.7K, 1%
R857
22K R856
UB15
4V REF
18.2K,1% R853
10K, 1% R855
15µf C807
TL084
T1 T2 T3 T4 T5 T6
U805
4051
OUT
+5
-12
U814
4053
REF
U815
TL084
.022 POLY C806
2.43K, 1% R852
1K 1% R851
U810
LS374
BD7 BD6 BD5 BD4 BD3 BD2 BD1 BD0
U807
FAST*
MSB
LSB
U8 1
3140
U809
LS374
30pf C804
U812
TL081
1.5K R841
U814
FTSH
U815
TL084
.022 POLY C805
30.1K 1% R849
13.4K,1% R850
U819
4053
22K R848
D804
33pf C808
NRES*
+5V
D802
D803
150Ω R844
100µF C802
10K 1% R846
10K, 1%, R845
U813
TL081
DAC

HIGH RESOLUTION DAC:

The Xpander uses a 14 bit DAC which provides the high resolution needed for the generation of smooth and accurate modulations. However an even higher resolution is required to achieve the very high standard of tuning accuracy that Oberheim likes to offer. This is accomplished by the circuitry on the right of the DAC U811 (see next page.)

Whenever a control voltage requiring a very high level of resolution (VCO or VCF frequency control) must be generated, this voltage will be obtained in two phases.

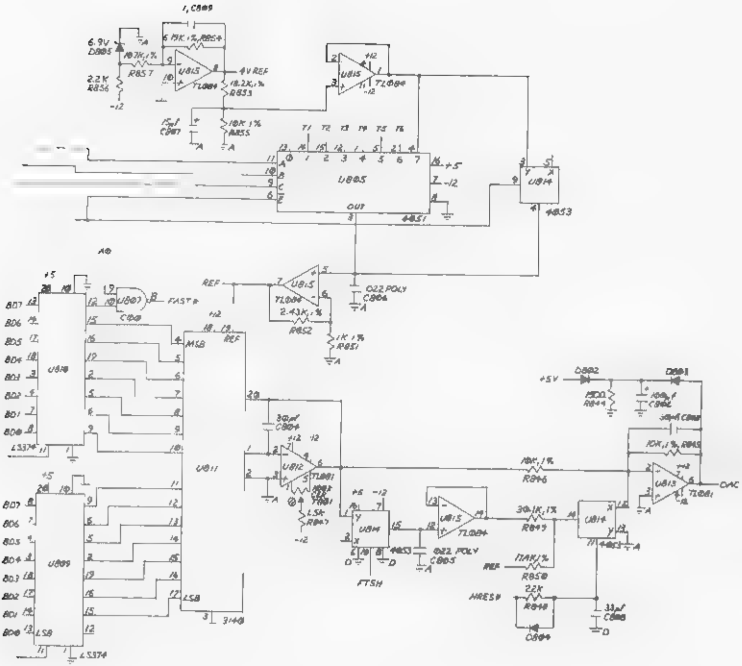
1) The DAC is first loaded with the fine tune value which is stored in the sample and hold formed by U814, C805 and L815.

2) The previously mentioned sample and hold's input is then disconnected from the DAC and the DAC is loaded with the most significant part of the control value. At this moment L814 connects the output of U815 (pin 14) to the summing node of U813 making its output equal to the sum of the control value and the fine tune value previously stored in C805. Simultaneously, the final destination sample and hold is connected to U813 output and stores the final value.

As the summing resistor for the fine tune sample and hold is three times the value of the other summing resistors (R849 and R846), the resolution obtained from the fine tune sample and hold is three times better than the original resolution of the 14 bit DAC.

When a control voltage which does not require this extra resolution has to be loaded in a sample and hold, the connection between pin 14 and 12 of L814 is open and the S&H is loaded in one phase.

Note that when the very high resolution mode is used, R850 is connected to the summing node of U813 bringing its output down of approximately 5 volts. This allows the use of a -5 to +5 voltage range for the VCO and VCF frequency controls making the line noise proportionally smaller.



U815
U805
U814
U810
U809
U811
U812
U813
4V REF
REF
FAST
FTSH
DAC
+5V
LS374
4851
4053
TL084
TL081
MSB
LSB
.022 POLY
BD7
BD6
BD5
BD4
BD3
BD2
BD1
BD0

VCO AND VCF FREQUENCY TUNING.

The volts per octave (scaling) parameters of the Xpander's 12 VCOs are adjusted by the voice microprocessor whenever the VCO function is selected in the tune page

By using the timer U921, the microprocessor mesures successively the five following frequencies C4, E5, G#6, C8 E9 for each VCO, and calculates the proper correction voltages to bring each oscillator in tune These correction values are stored in the main processor's battery back up memory for instant recall upon power on

During normal operation, whenever a VCO will be required to produce a E5 for example, the correction value for this VCO at this frequency will be added to it's control voltage For the notes between the sampled frequencies, the voice microprocessor calculates a linear interpolation from the two adjacent correction values and a linear extention from the two last values for the notes under C4 or over E9

After the VCFs have been set to oscillation by setting the resonance controls at maximum, their frequencies are tuned like the VCO frequencies

PULSE WIDTH CALIBRATION:

The 50 percent duty cycle of the Xpander's12 pulse width modulators are adjusted by the voice microprocessor whenever the PW function is selected in the tune page

By using the timer U921, the microprocessor meaSures the duty cycle for each pulse width modulator, and calculates the proper correction voltages to bring them to 50 percent for a control value of 31 These correction values are stored in the main processor's battery back up memory for instant recall upon power on

FILTER RESONANCE CALIBRATION: for voice software version 1.1

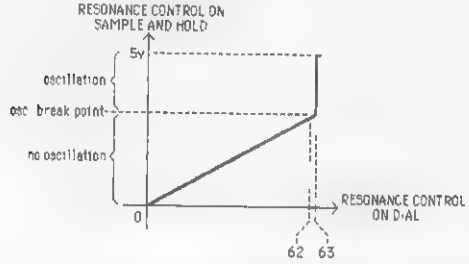
Every time the RES function is selected in the tune page, the voice microprocessor performs the following tests

1 The software checks that the filter is oscillating when its frequency is set for E9, and its resonance control is at maximum (5 volts) This test insures that the VCF will be able to oscillate over the keyboard range

2 The filter frequency is set for E5 and the resonance control is decreased until the filter stops oscillating

3 The resonance is slowly increased until the filter starts oscillating again The resonance value at this point is saved as the "oscillation break point"

During normal operation the microprocessor scales the resonance control as shown on the figure below



As the frequency of the CEM 3372 changes slightly with its resonance setting, the VCF frequencies are automatically retuned after the resonance calibration has been performed

DUAL VCO CEM 3374:

The CEM 3374 contains two completely independent precision voltage controlled oscillators. The 3374 includes an on chip temperature sensor which generates an output voltage, nominally +2.5V, proportional to the chip temperature with a T.C. of +3300 ppm.

CEM 3374 BLOCK DIAGRAM

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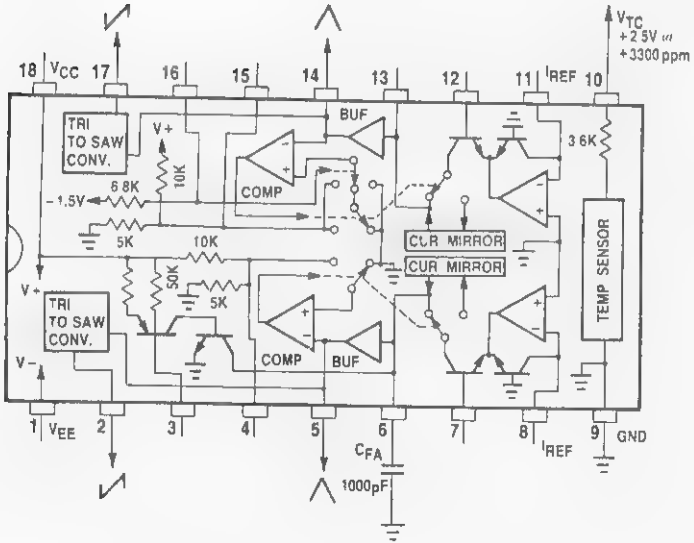

SIGNAL PROCESSOR CEM 3372:

The CEM 3372 is an audio signal processing device It includes a two channel voltage controlled mixer, a dedicated 4-pole low pass VCF with voltage controlled resonance and a final VCA With the exception of the filter cut-off frequency, all control inputs are very low bias current, high impedence which range from 0 to 5 volts

CEM 3372 BLOCK DIAGRAM

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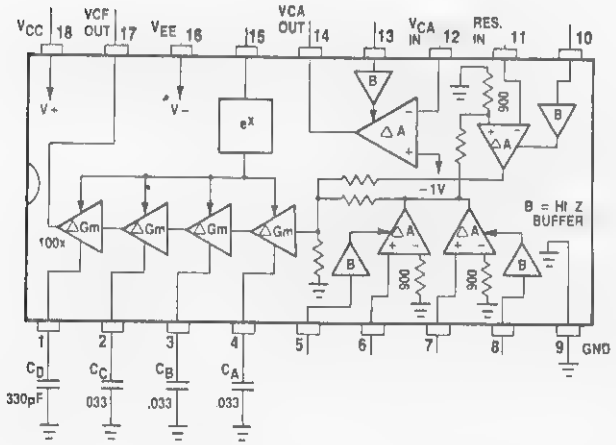


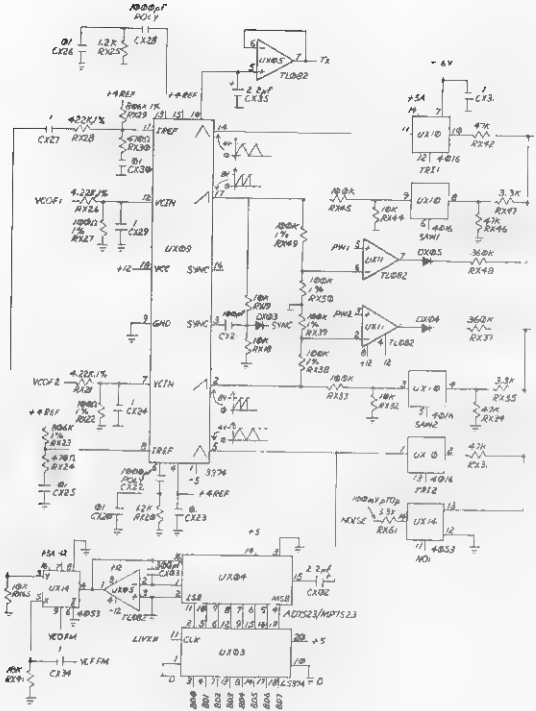
DYNAMIC FM IMPLEMENTATION:

The Xpander voice allows dynamic linear modulation of VCO1 frequency by VCO2 triangle output.

This is done by sending the triangle output of VCO2 (pin 5 of UX09) to the reference input of the multiplying DAC UX04 which has its combination inputs controlled by the latch UX03. The op amp UX05 converts the current output of the DAC into a voltage.

The three IC's mentioned above act as a digitally controlled variable gain amplifier where pin 15 of UX04 is the amplifier input, pin 1 of UX05 is the amplifier output and pin 4 through 11 of UX04 are the digital gain control inputs. The analog switch LX14 routes the modulation signal either to the linear frequency control input of VCO1 (pin 11 of UX09) or to the VCF frequency input (pin 15 of UX12).

This method is preferred over using a conventional VCA because of the much better temperature independancy and linearity of the multiplying DAC.

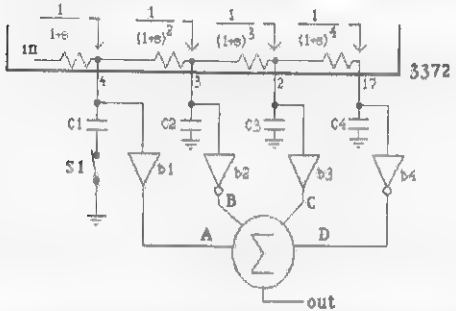


MULTI FUNCTION VCF:

Although the VCF implemented in the 3372 is a standard 4-pole low pass the additional circuitry made of UX14 UX13 UX15, UX17, and the one percent resistor array on the left of JX17 allows 15 different filter modes including high pass, band pass, notch and all pass

Understanding how this magic trick happens requires a little theory

The figure below shows a simplified representation of the circuitry



The complex representation of the transfer function of a 1-pole low pass filter is = $\frac{1}{1+s}$ Therefore, the transfer function of the network will be

$$\frac{out}{in} = \frac{A}{1+s} - \frac{B}{(1+s)^2} + \frac{C}{(1+s)^3} - \frac{D}{(1+s)^4} = \frac{As^3 + (3A-B)s^2 + (3A-2B+C)s + A-B+C-D}{(1+s)^4}$$

Selecting specific values for A, B, C and D allows differente transfer functions For exemple, selecting A=1 B=1, C=0 and D=0 transforms the above equation into

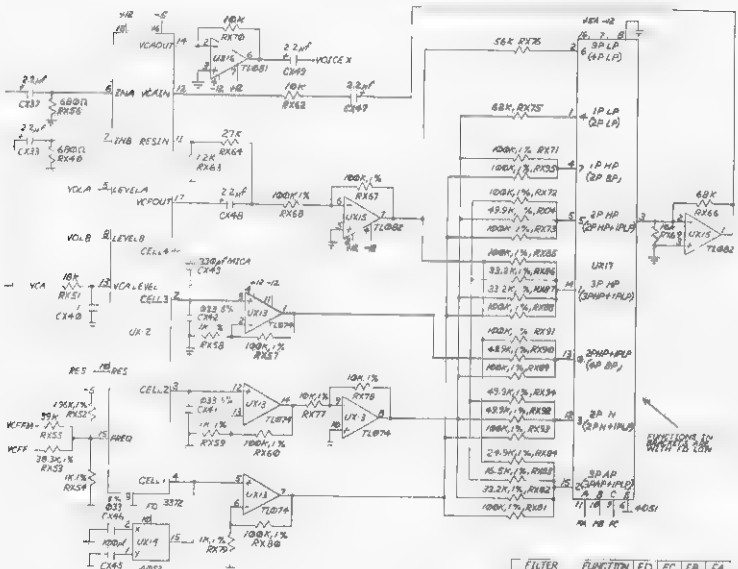
$$\frac{s}{(1+s)^2}$$

which is the transfer function of a 2 pole band pass filter

Getting different responses from this network will be just a matter of adjusting the coefficients A, B, C and D in order to transform the transfer function into the desired one

For the high pass and all pass filter modes, it is necessary to cancel the first cell of the filter This is accomplished by opening the switch S1

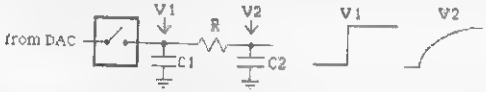
n practice S1 is implemented by one cell of the analog switch UX15, the buffers b1, b2 and b3 are the four op amps of UX13, b4 is the op amp UX15 (output pin 7) and the summation is performed by the second cell of UX15 (output on pin 1). The coefficients A, B, C and D are set by the value of the summing resistors. The analog multiplexer UX17 allows to select from eight different resistor combinations providing eight different filter modes. Seven additional modes are obtained by selecting the previous modes and opening S1.



FILTER	FUNCTION	FD	FC	FB	FA
4P BP		0	0	0	0
3P NP + 1PLP		0	0	0	1
3P AP + 1PLP		0	0	1	0
2P N + 1PLP		0	0	1	1
2P LP		0	1	0	0
2P HP + 1PLP		0	1	0	1
4P LP		0	1	1	0
2P BP		0	1	1	1
2P HP + 1PLP		1	0	0	0
3P NP		1	0	0	1
3P AP		1	0	1	0
2P N		1	0	1	1
NP LP		1	1	0	0
2P HP		1	1	0	1
3P LP		1	1	1	0
1P HP		1	1	1	1

SMOOTHING SAMPLE AND HOLD:

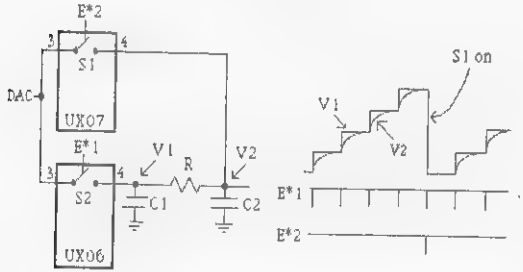
Most of the modulations in the Xpander are generated by the voice micro processor and are transmitted to the analog part of the voice through the DAC and sample and hold. Every 10 ms, the processor computes a new value of the modulation and updates the corresponding sample and hold. Without any special attention in the design of the sample and hold, this would produce a step in the control voltage every 10 ms. To avoid this problem, the Xpander S&H use a circuit which allows smoothing of the transition between successive samples. This is done by adding an RC network after the sample and hold capacitor C1.



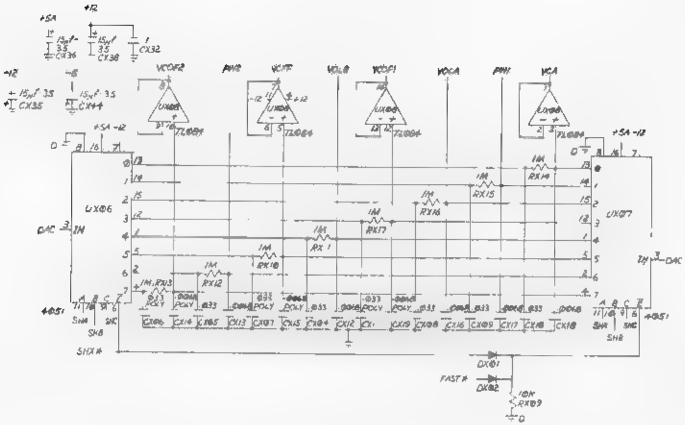
Because C1's value is much larger than C2, it acts as a voltage generator for the 10 ms time interval between refresh.

It is, however, necessary for some specific modulations, such as an LFO with a sawtooth wave, to cancel this RC time constant in order to produce the sharp edge of the wave. This is done in practice by short-circuiting the resistor R.

The figure below shows one of the eight sample and holds of a voice with a slightly different placement of the components.



If a smooth transition is required, S2 is switched on while S1 remains open. For a sharp transition S2 and S1 are closed simultaneously.

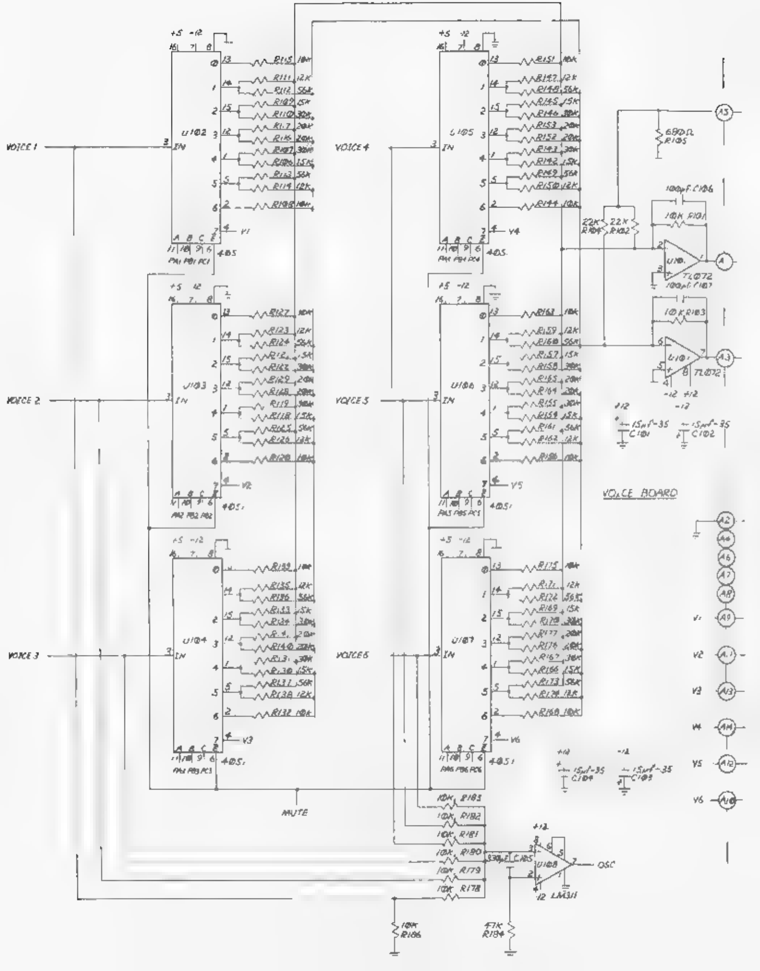


+5A
+12
CX36
CX38
CX32
CX35
CX44
VCOF2
VCF
VCOF1
VCA
UX06
UX07
DAC
IN
TL084
4051
SHA
SHB
SHC
SHX#
FAST#
DX01
DX02
10K
RX09
RX12
RX15
RX16
RX17
POLY

PROGRAMMABLE PANNING:

The programmable panning is implemented by the IC's L102 through L107

The output signal of a voice is routed to one of the eight outputs of its associated IC The one or two resistors connected to this point distribute the signal to the left and right audio bus The eighth output is connected to the direct output feedback The enable inputs of those ICs (pin 6) allow muting of all the outputs during the tuning


VOICE 1
VOICE 2
VOICE 3
VOICE 4
VOICE 5
VOICE 6
U102
U103
U104
U105
U106
U107
U108
LM311
TL072
MUTE
OSC
VOICE BOARD

TEST AND CALIBRATION:

The only equipment required to perform the Xpander test and calibration are a well calibrated digital voltmeter (DVM) with 4 1/2 digit resolution and a sound system

POWER SUPPLY TEST:

1. Attach the negative lead from the DVM to the ground lug on the voice board at the left of the DAC

2. Set the DVM for: DC volt, range 10v
   With the positive probe, test the 6 following voltages at the power supply connector on the voice board

+12	+/- 750 mv	(11.250v	to	12.750v)
-12	+/- 750 mv	(-11.250v	to	-12.750v)
-5	+/- 500 mv	(-4.500v	to	-5.500v)
+5A	+/- 500 mv	(4.500v	to	5.500v)
+5D	+/- 500 mv	(4.500v	to	5.500v)
ANGD 0v	+/- 10 mv			

3. Check the +5M (+5 MEMORY) on the right lead of D4 located at the middle top of the processor board

With power ON	4.4v	+/- 600 mv	(3.80v to 5.00v)
With power OFF	2.7v	+ 1.3v /- 300 mv	(2.40v to 4.00v)

4. Set the DVM for: DC volt, range 100v.
   Check the 55v on pin 6 of the power connector of the pot board

55v	+/- 4v

5. Set the DVM for: AC volt, range 10v.
   Check the 9v AC between pin 7 and 8 of the power connector on the pot board

9v AC	+/- 2v

NOTE The AC frequency at this point is approximately 30 KHz Make sure that your AC DVM reading is valid for this frequency range, if not, use an oscilloscope

MAIN PROCESSOR ROM AND RAM TEST:

1 Turn the memory protect swith off on the back panel
2 Select MASTER PAGE
3 Select PAGE 2
4 Select SERVICE
5 Select MEM
6 Check for the following succesive messages

RAM 0 OK
RAM 1 OK
RAM 2 OK
ROM 0 OK
ROM 1 OK
ROM 2 OK
ROM 3 OK

If one of the test fails (RAM or ROM X BAD) replace the corresponding chip RAM 0 = U2, RAM 1 = U3, RAM2 = U4, ROM 0 = U8, ROM 1 = U7, ROM 2 = U6, ROM 3 = U5

VOICE PROCESSOR ROM AND RAM TEST:

1 Select MASTER PAGE
2 Select PAGE 2
3 Select SERVICE
4. Select VMEM
5 Allow 20 seconds delay and check for message "CA MEM OK"

If the test fail (CA MEM BAD), replace successively U912, U914, U917 until the test run succesfully.

LEDs TEST:

1. Select MASTER PAGE.
2 Select PAGE 2
3 Select SERVICE.
4 Select LED
5 Check for all 16 LEDs lit for approximatly 2 seconds
Check then for all LEDs lighting one after each other one at a time

VACUUM FLUORESCENT DISPLAY TEST.

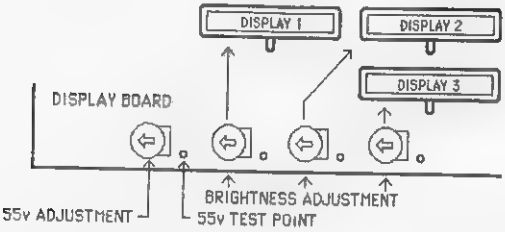
1 Select MASTER PAGE
2 Select PAGE 2
3 Select SERVICE
4. Select DISP
5. Check for all segments ON for all 120 digits
Check for all segments ON for 1 digit at a time
Check for 1 segment ON at a time for all digits of display 1, then display 1 &2, then display 1,2 & 3.

VFD BRIGHTNESS ADJUSTEMENT:

1 Set the DVM for: DC volt, range 100v

2 Adjust the 55v

55v +/- 4v



3 Turn the three brightness trimmers all the way up (maximum brightness)

4 Turn down the trimers of the brightest displays to match the dimmest one

4 VOLT REFERENCE TEST:

1 Attach the negative lead of the DVM to the ground lug on the voice board at the left of the DAC

2. Set the DVM for: DC volt, range 10v.

3 With the positive probe check the 4 v reference voltage on pin 8 of U815 (TL084) in the DAC area of the voice board

3.920v < 4v ref < 4.080v (4v +/- 2%)

DAC CALIBRATION:

1. Set DVM for: DC volt, range 10v

2 Attach the negative lead from the DVM to the ground lug on the voice board at the left of the DAC

3. Select MASTER PAGE

4. Select PAGE 2

5 Select SERVICE.

6. Select DAC OFFSET

7 With the positive probe of the DVM, check the output voltage of the DAC on pin 6 of U812 (TL081) and adjust with DAC trimer TB01 for

0v +/- 1 mv

NOTE The IC U814 (4053) in the DAC area is very sensitive to short circuit Be very careful when testing pin 6 of U812

DAC MONOTONICITY TEST:

1. Select MASTER PAGE.
2. Select PAGE 2.
3. Select SERVICE.
4. Select DAC MONO.
5. Check for no or very seldom beep on the audio output.

ANALOG TO DIGITAL CONVERTER CALIBRATION:

Note: This calibration is going to set the volt per octave of the CV in. It is assumed that the controlling CVs are in the range 0 to 5 volt, that they are set for 1volt per octave +/- .2% with a linearity of at least .1% and that the offset is no more than +/- 15 mv. If the controlling device does not fulfill these requirements it will have to be corrected.

A) DVM METHOD: (calibration relative to internal DVM reference)

1. Set the DVM for: DC volt, range 10v

2. Attach the negative lead of the DVM to the ground reference of the ADC on the left side of R65 (10 Ohm) on the pot board.

3. With the positive probe of the DVM, test the ADC reference voltage (pin 9 of U20) on the lower lead of R47 on the pot board. Adjust with trimer T1 for:

2.667v +/- 2mv (2.665v to 2.669v)

B) AUDIO METHOD: (Calibration relative to the CV generator reference)

1. Select a single patch appropriate for checking voice tuning.

2. Set voice 1 and 2 to be controled by CV 1 and CV 2.

3. Supply simultaneously CV1 input with 0.000 volt and CV2 with 5.000 volt. Gate voice 1 and 2 (Using a well calibrated DSX is one way to do it).

5. Adjust trimer T1 to obtain two stable notes C0 and C5.

MISCELLANEOUS:

SOFTWARE RESET:

In case of program lockup or abnormal software behavior, you can reset the memory of the processors to an initial default configuration.

To do so;

1. Hold down the CLEAR switch (most right switch in the modulation source select area) while you turn the power on.
2. Select YES under display 3. (selecting NO will cancel the reset).

The patch memory remains unaffected by this operation.

SOFTWARE VERSION NUMBER:

You can find out the software revision numbers actually installed in an Xpander by:

1. Select MASTER PAGE.
2. Select PAGE 2.
3. Select VERSION.

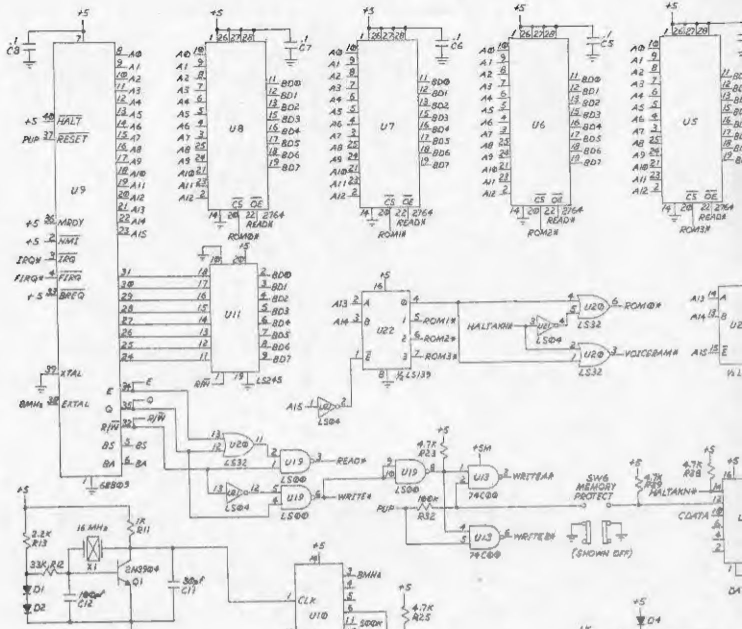
UNTUNE:

You can cancel all the automatic correction (VCO, PW, RES, VCF tuning) by:

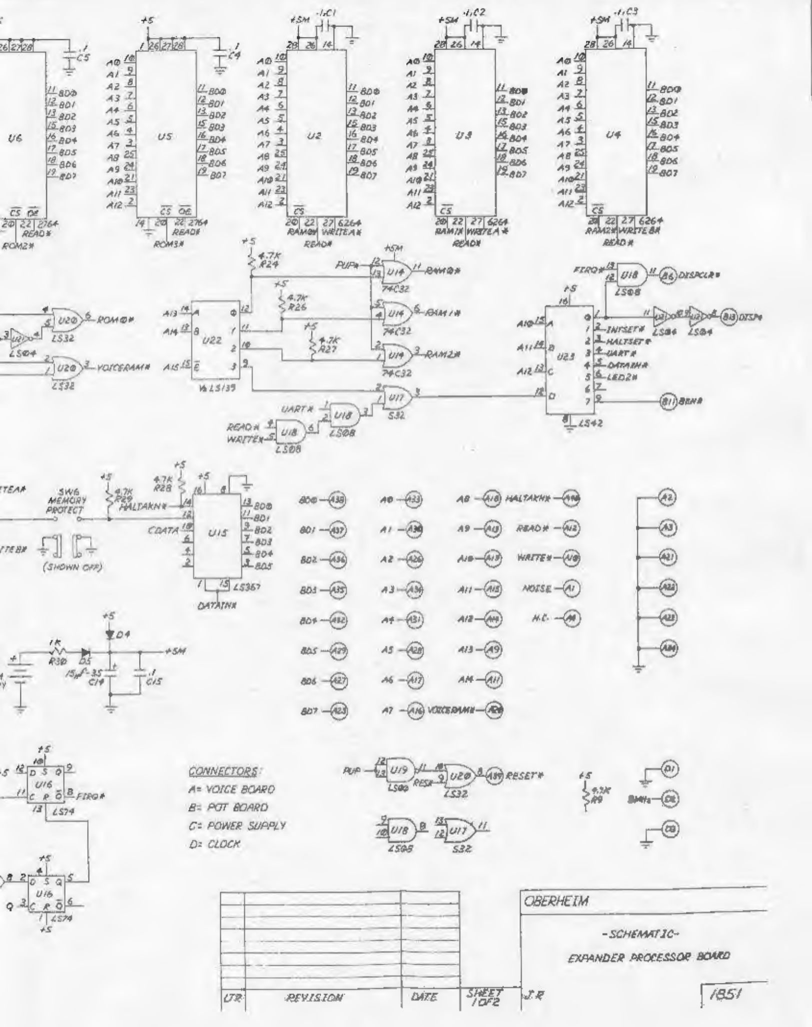
1. Select MASTER PAGE.
2. Select PAGE 2.
3. Select SERVICE.
4. Select UNTUNE.

All the correction parameters will be set to 0. This may be useful when for example you wish to find out how much apart the resonance control of two VCFs really are, or if you want to check the linearity of a sample and hold ... etc.

To retrive the tuning parameters, do a tune all in the TUNE PAGE.



U9
68B09
HALT
RESET
MRDY
NMI
IRQ
FIRQ
BREQ
XTAL
EXTAL
8MHz
PUP
IRQ#
FIRQ#
C8
U8
U7
U6
U5
2764
READ#
ROM0#
ROM1#
ROM2#
ROM3#
C7
C6
C5
U11
LS245
R/W
U22
1/2 LS139
HALTAKN#
U21
LS04
U20
LS32
VOICERAM#
A15
READ#
WRITE#
U19
LS00
R23
4.7K
+5M
U13
74C00
WRITEA#
WRITEB#
SW6
MEMORY
PROTECT
(SHOWN OFF)
R32
100K
R29
4.7K
R38
CDATA
2.2K
R13
16 MHz
X1
1K
R11
33K R12
2N3904
Q1
D1
D2
100pF
C12
30pF
C11
U10
CLK
800K
LS393
R25
B1
2.9V
LITHIUM
BATTERY
R30
D5
D4
15µF-35
C14
C15
8 X 4.7K
U1
LS374
INTSET#
U12
40103
U16
LS74
U17
S32


CONNECTORS:
A= VOICE BOARD
B= POT BOARD
C= POWER SUPPLY
D= CLOCK
SW6 MEMORY PROTECT
(SHOWN OFF)
OBERHEIM
-SCHEMATIC-
EXPANDER PROCESSOR BOARD
LTR
REVISION
DATE
SHEET 1 OF 2
J.R
1851